Shock Performance Study of Solder Joints in Wafer Level Packages

Amarinder Singh Ranouta[1], Xuejun Fan[1, 2], Qiang Han[2]
[1]Department of Mechanical Engineering
Lamar University
PO Box 10028, Beaumont, TX 77710, USA
[2]College of Civil Engineering and Transportation
South China University of Technology, Guangzhou, China
xuejun.fan@lamar.edu

Abstract

In this paper, an integrated testing, finite element modeling and failure analysis approach for drop test reliability of wafer level packages is developed to examine the shock performance of large array wafer level packages. For standard JEDEC drop test, it has been found that corner component group (group A) failed first for 12×12 array packages. This is different from previously reported failure test data of BGA packages. Careful analysis concluded that the high failure rate of group A is mainly due to the effect of mounting screws rather than the intrinsic strength of the package. For a given WLP, corner balls always fail first during drop test. The crack initiates at inner side of the solder joint and propagate towards the opposite side. The primary failure is always on the intermetallic compound (IMC) at WLP side. It has been found that drop reliability significantly decreases with array size increasing. Novel finite element modeling approach has been developed to correlate with experimental data. The finite element model was validated with experimental board strain data, and frequency analysis. In-plane principal strain at corner locations and maximum peeling stress in IMC at critical solder joints are used to correlate with experimental data. Excellent agreement was reached to predict the failure rate of components in each group. Two new findings have been observed and validated. One is that existing JEDEC board design will lead group A components fail first for certain array size of wafer level packages. Another finding is that PCB board strain does not always correlate with maximum peeling stress in solder joints when array size changes.

1. Introduction

Reliability of handheld electronic devices such as cellular phones due to drop and impact event is a major concern in electronics industry. During a drop/impact event, printed circuit board (PCB) assembly inside casing vibrates causing a flexural/bending motion of the board [1]. The PCB bending results in transient dynamic stresses or strains on solder joints of electronic components. It ultimately leads to the failure in solder joints. The failure can occur at package side or PCB side. Other failure modes such as pad-crater and broken board traces are also observed [2].

The dynamics and reliability of electronic components under board level drop test have been well studied. A board level drop test method has been standardized through Joint Electronic Device Engineering Council (JEDEC), JESD22-B111 (2003) [3], to evaluate the performance of IC packages under drop conditions. Multi-channel real-time monitoring system has been applied to record electrical connections of daisy-chained components, accelerations, and in-plane strains at various locations of PCB using strain gages and accelerometers [4-7]. High speed cameras have been applied to capture the images of board assembly during impact to extract displacement and deformation [7-11]. Digital Image Correlation (DIC) system integrated with the cameras has been developed to analyze the acquired images to give dynamic deformation, shape and strain over the entire surface of board [8-16].

Previously, various shock/impact modeling techniques have been developed to predict board dynamic strains and transient solder joint stresses. Explicit dynamics has been applied in both product and board levels [7-11 and 17-19]. Several special treatments such as equivalent layer models for solder interconnects [11], shell element in global models [20], solid-to-solid sub-modeling technique using half PCB board [21-23], shell-to-solid sub-modeling using beam-shell-based quarter symmetry models [8-11 and 17], shell-to-solid sub-modeling without any assumption of symmetry [9-11], have been developed to reduce the computational time required for simulation. The board level model can be analyzed by using the drop table acceleration as input loading. This so-called Input-G method decouples the board finite element model from the system model [24]. There are several approaches in implementing the input-G loading method. Tee used explicit dynamics analysis by directly applying acceleration impulse using DYNA-3D [7]. Syed introduced the large mass method to convert acceleration input into force input by multiplying the acceleration with a large mass with implicit dynamics [20]. Irving proposed the input-D method, in which the acceleration input is integrated twice to obtain the displacement boundary condition over time [25]. Loh used mode superposition method for a linear system under impact loading [5].

In this paper, a comprehensive study is carried out to examine the shock performance of large array wafer level packages (WLPs). Copper post wafer level packages are used with different array sizes to investigate the failure characteristics under JEDEC setting. Experimental work for controlled JEDEC drop test is conducted. It is found that the primary failure mechanism of WLP drop test failures is fracture of intermetallic compound (IMC) at WLP side. Transient board strains and accelerations at various locations are measured during impact to correlate with failure life of each component. The fundamental frequencies of test board are extracted through FFT transformation. Statistical analysis is performed to analyze the drop life for each group. Finite

element modeling using newly developed direct acceleration input method (DAI) is applied. Global/local modeling is adopted to capture both board strains and solder joint stresses accurately. Experimental results are compared to the simulation data. The effects of array size and failure locations are studied in detail. The correlation between board strain and solder joint stress is described. Several new findings through both test and simulation are discussed.

2. Experimental Setup [6]

In this study, a JEDEC test board has been used with dimensions 132mm×77mm×1mm. The test board has 15 copper post wafer level packages with different array sizes. The packages are populated on one side in a three-row, five-column format, as shown in Figure 1.
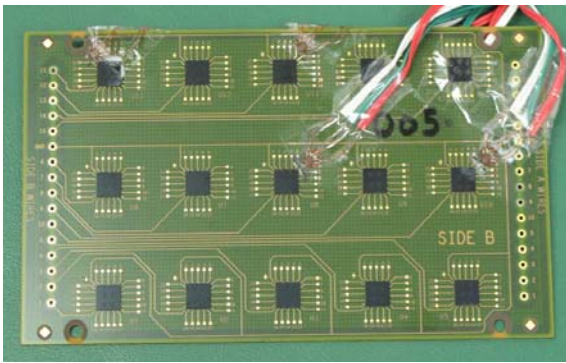
Figure 1 JEDEC test board and strain gauge rosette attachments

Figure 2 is a schematic view of solder bump structure for a copper post wafer level package. A thick copper post, which is encapsulated by epoxy, is formed on wafer level before ball attachment. The geometric dimensions of the WLP are given in Table 1. The ball pitch is 0.5mm. The test assemblies have been subjected to a 1500g, 0.5ms pulse consistent with the JESD22-B111. The drop height and the pulse shape have been adjusted using pulse shapers between the impacting surfaces. A half-sine pulse has been achieved. Figure 3 shows the schematic of shock test platform, acceleration profile of shock table, and the arrangement of components (face-down) and numbering.

Table 1 Geometrical dimensions of copper post WLP

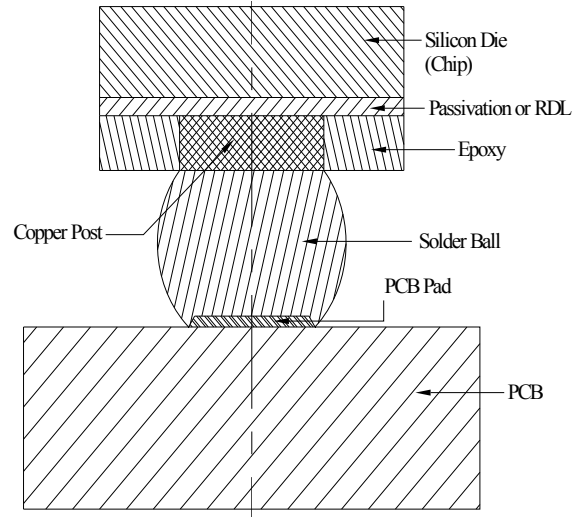|	Dimensions (μm)
Silicon thickness	400
Solder ball diameter	310
Solder ball standoff height	240
Solder ball opening diameter	250
PCB pad diameter	250
PCB thickness	1000
Wafer Passivation thickness	4
Epoxy/Copper post thickness	70

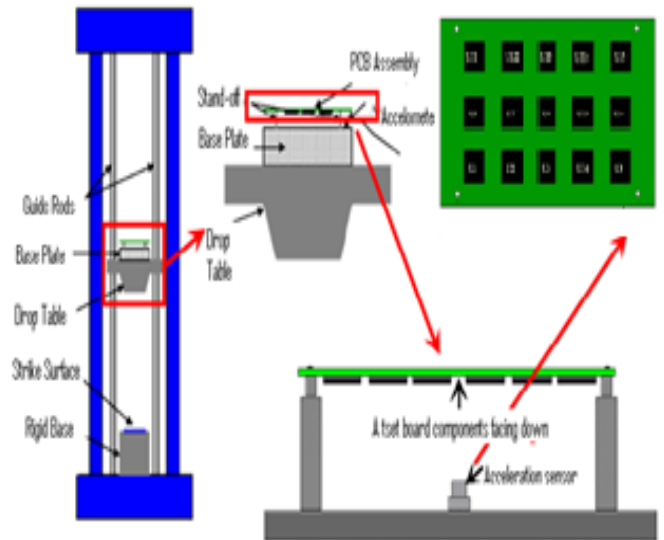Figure 2 Cross-section view of solder bump structure for a copper post wafer level package

Figure 3 Schematic of experimental setup for controlled JEDEC drop test

45° strain gauge rosettes, which are attached with 1mm offset from component corner in both horizontal and vertical directions as per IPC9704 at U8, U10 and U15 locations, respectively (as shown in Figure 1), are used to measure board strain transient responses. A typical strain data measurement is given in Figure 4 for the central component U8 at 0°, 45°, and 90°, respectively [6]. Frequency spectrum of board vibration is generated a by strain data through fast Fourier transform (FFT). Figure 5 shows the frequency spectrum of PCB strains. As is seen the first resonant frequency is registered at 230Hz, and second one is found at ~ 650Hz.
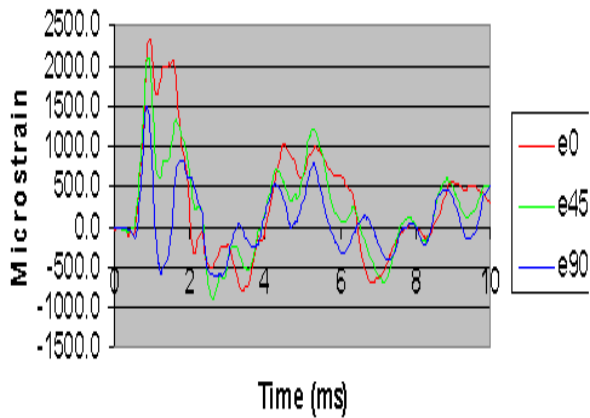
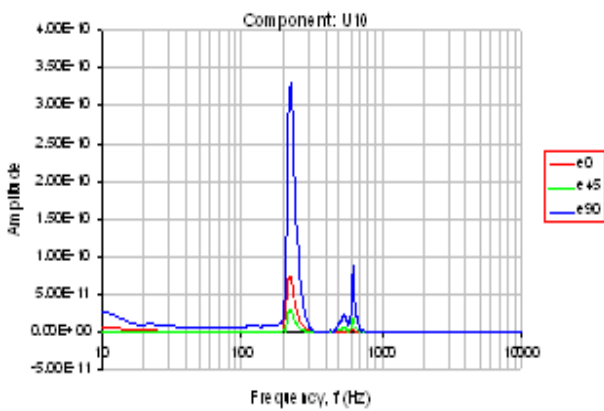Figure 4 Strain components as function of time at U8 location

Figure 5 Frequency spectra through FFT

3. Finite Element Modeling

There are 15 components on a JEDEC board and each component has hundreds of solder balls. In order to handle this very large model without sacrifice of accuracy, special considerations are implemented in both global and local model levels. In global model, a quarter model is created due to symmetry. Solder balls are simplified as rectangular blocks with one 3-D solid element for each ball. Copper post, epoxy, passivation layer, and PCB pad are neglected in the global model, as shown in Figure 6. 3-D elements are used for entire structure including PCB board and silicon chips. Direct acceleration input (DAI) method is used to apply impulse loading [21-23 and 26]. The damping coefficient for PCB is determined by correlating with experimental strain data (to be discussed in next section).

A local model is constructed next. The script is developed to build a local model at any desired location of components. Figure 7(a)-(c) show an example of a local model for component U1. In the local model, the PCB is extended to 2mm away from component corner in both x and y directions, respectively to create cut boundary and DOF constraints taken from global model.

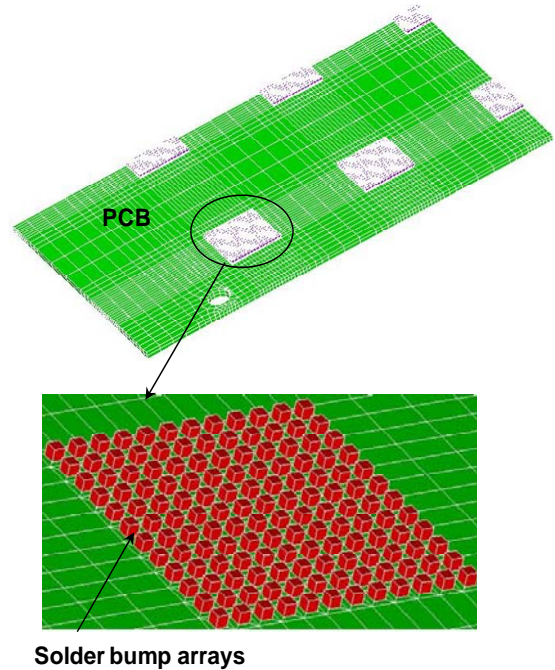**PCB**

Solder bump arrays

Figure 6 A quarter global finite element model

In order to further reduce the model size, all solder balls in the local model are modeled as rectangular blocks, except critical solder balls with refined meshes and detailed structures. It has been shown that such a local model can produce almost same results compared to a local model with all refined solder balls [21-23]. Figure 7(d) and 7(e) describe the details of solder ball structures in the local model with rectangular blocks and refined structures, respectively. Since the primary failure is at the intermetallic layer on WLP side [6], a 10μm layer with two layers of elements is created at solder/copper post interface.

Table 2 defines the material properties used for both global and local finite element models. All the materials are considered as elastic ones.

Table 2 Material Properties

Material	Mechanical Properties		
	Modulus (GPa)	Poisson Ratio	Density (gm/cm^3)
PCB	22	0.25	2.1
Solder (SAC)	51	0.36	7.2
Silicon Die	130	0.278	2.5
Underfill	10	0.3	2.0
Copper Post	128.8	0.34	8.3
Epoxy	4.7	0.38	2.2
Passivation	2.89	0.34	2.2
PCB Pad	128.8	0.34	8.3

(a) Global model

Cut boundary

Cut boundary
DOF constraints at 2mm×2mm
from package corner

(b) Local model

(c) Solder ball meshes in local model

Silicon

Epoxy

Copper post

Solder ball

PCB

(d)

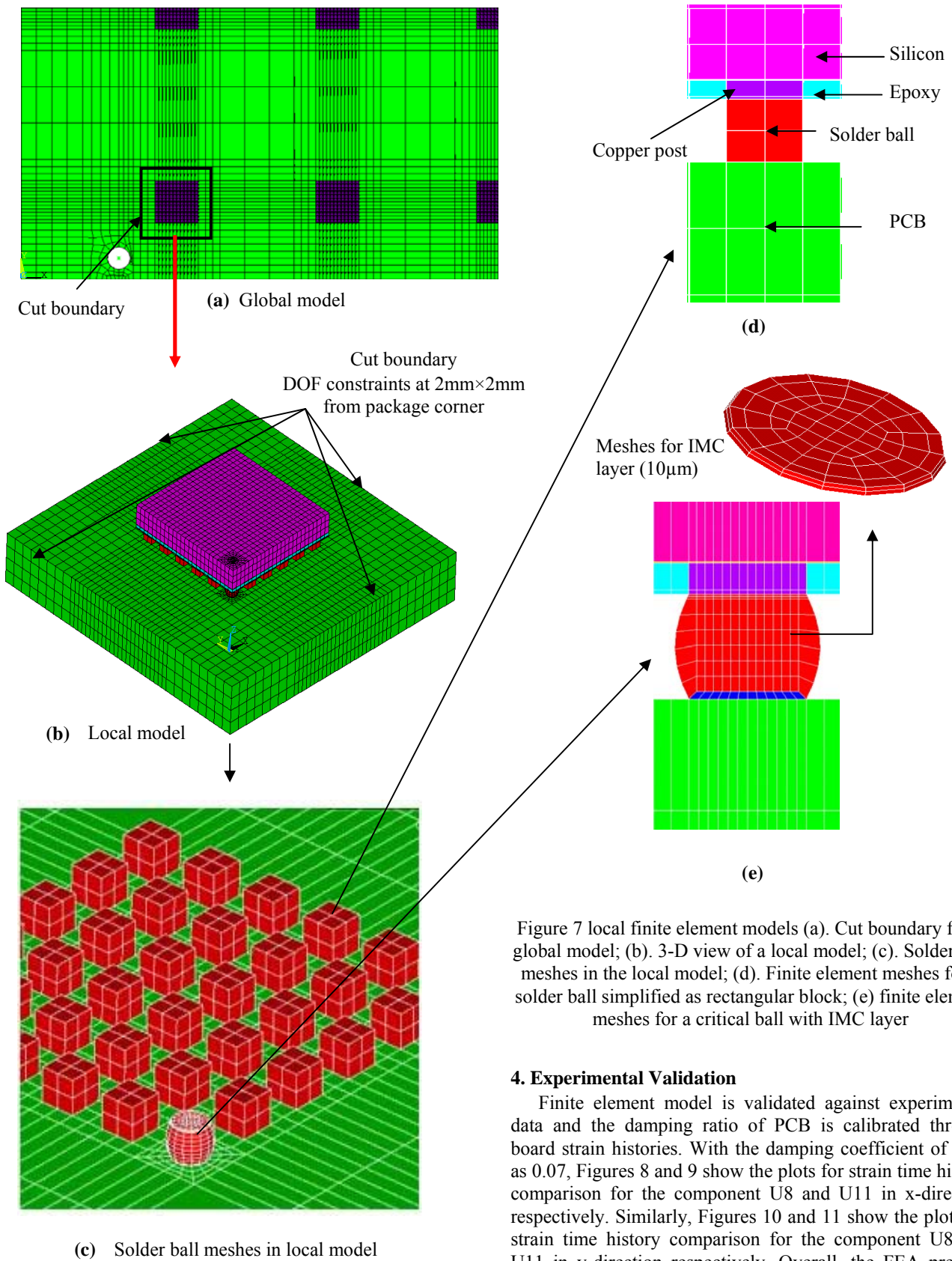Meshes for IMC
layer (10μm)

(e)

Figure 7 local finite element models (a). Cut boundary from global model; (b). 3-D view of a local model; (c). Solder ball meshes in the local model; (d). Finite element meshes for a solder ball simplified as rectangular block; (e) finite element meshes for a critical ball with IMC layer

4. Experimental Validation

Finite element model is validated against experimental data and the damping ratio of PCB is calibrated through board strain histories. With the damping coefficient of PCB as 0.07, Figures 8 and 9 show the plots for strain time history comparison for the component U8 and U11 in x-direction respectively. Similarly, Figures 10 and 11 show the plots for strain time history comparison for the component U8 and U11 in y-direction respectively. Overall, the FEA predicts the board strain dynamic responses very well.
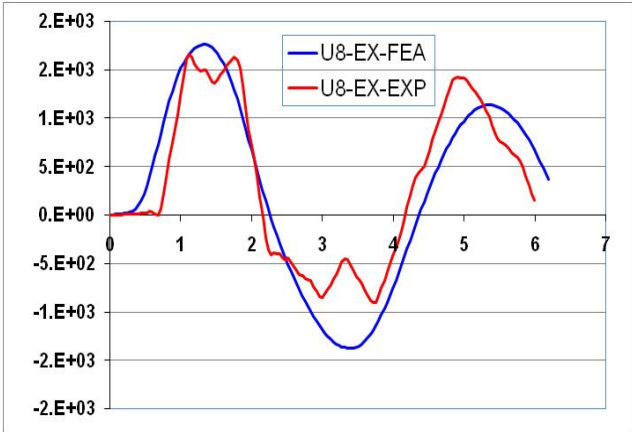
Figure 8 Strain time history comparison for experimental and FEA prediction for U8 in x-direction
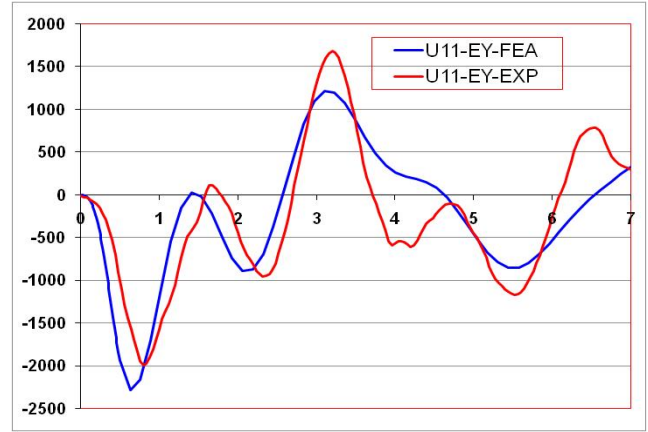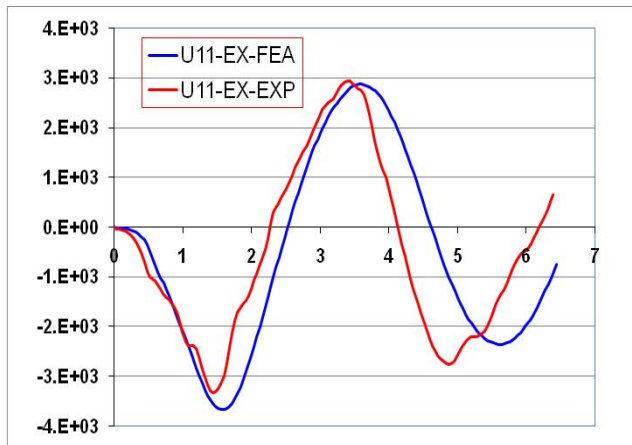

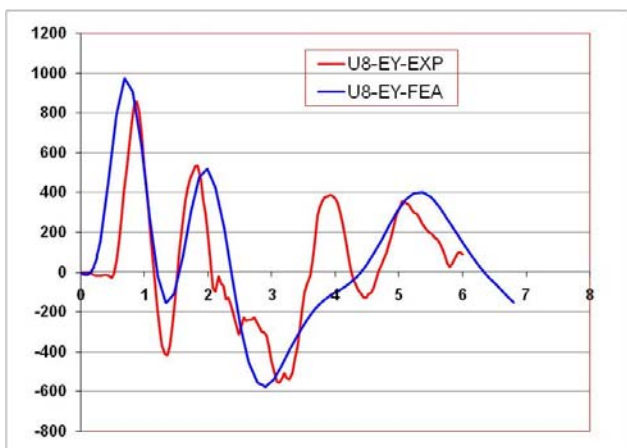Figure 9 Strain time history comparison for experimental and FEA prediction for U11 in x-direction

Figure 10 Strain time history comparison for experimental and FEA prediction for U8 in y -direction

Figure 11 Strain time history comparison for experimental and FEA prediction for U11 in y -direction

Modal analysis is also performed with the global finite element model. The first two symmetrical modes and the corresponding natural frequencies are calculated as 220Hz and 654Hz, respectively from modeling. It is seen that at fundamental frequency, the mode shape is ε_x dominant. While at 654Hz the mode shape is εy dominant. Modeling results correlate very well with measured data in Figure 5 (230Hz and 650Hz).

5 Board Strains Analysis

5.1 Corner Strain Analysis

Previous studies have shown that board strains at package corner locations can correlate well with solder joint failures [5]. In the following study, the exact corner locations on component side are picked for strain data evaluation. In other words, corner strains in the following are defined as strains on PCB at component side at the exact left corner location for each component. ε_x, ε_y, and ε_{xy} can be extracted from finite element results. In-plane principal strain ε_1 and ε_2 can be calculated as follows,

$$\varepsilon_{1,2} = \frac{1}{2}\left[(\varepsilon_x + \varepsilon_x) \pm \sqrt{(\varepsilon_x + \varepsilon_x)^2 + \gamma_{xy}^2}\right] \tag{1}$$

where $\varepsilon_{1,2}$= Principal strains

ε_x = Strain in x-direction (PCB board long-side)

ε_y = Strain in y-direction (PCB board short-side)

γ_{xy}= Shear strain in x-y plane (board plane)

Since only positive board strain (component side) generates tensile stress in solder balls, the first principal strain ε_1 will be analyzed only. Figure 12 and Figure 13 plot the ε_x and ε_y time history for all components (U1, U2, U3, U6, U7, and U8) respectively. From these figures it is quite clear that ε_x is dominant for most components except U6, in which ε_y is dominant. In Figure 14, it is shown that the maximum principal strain at U6 occurs when the maximum ε_y is reached. At the same time, the ε_x is negative.
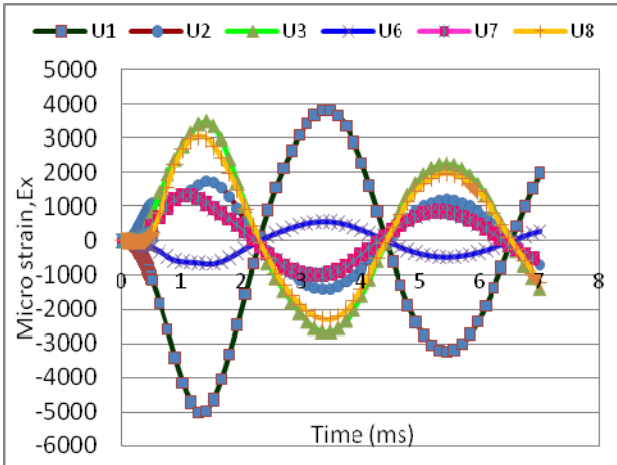
Figure 12 Strain time history plot for globl model of array 12×12 in x-direction

Figure 13 Strain time history plot for global model of array 12×12 in y-direction

Figure 14 Maximum principal strain at U6 and corresponding ε_x and ε_y (12×12 array)
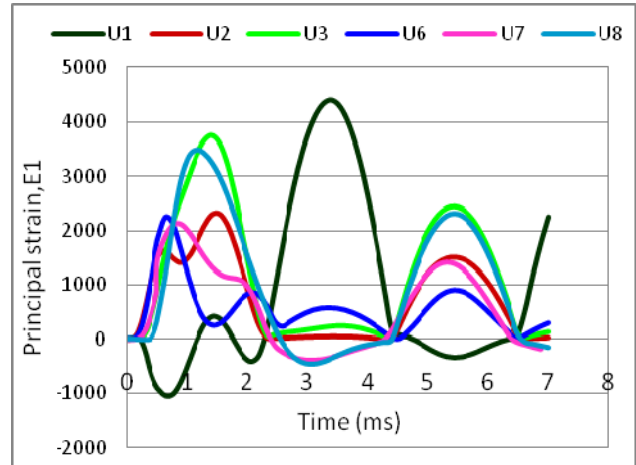

Figure 15 Principal strain history plot (12×12 array)

Figure 15 plots the principal strain ε_1 history. It is clear that U1 has the maximum board strain among all components, followed by U3 and U8.
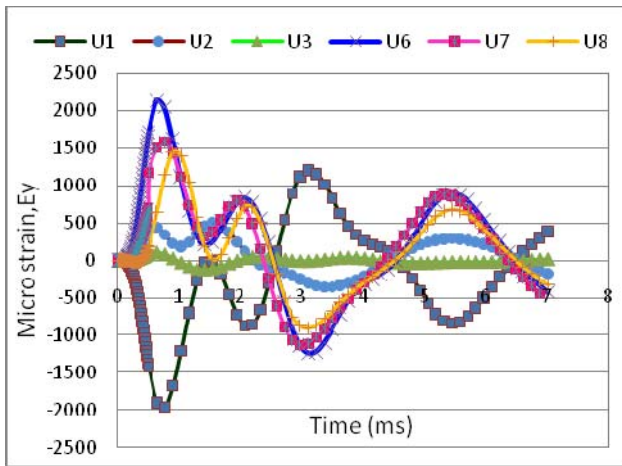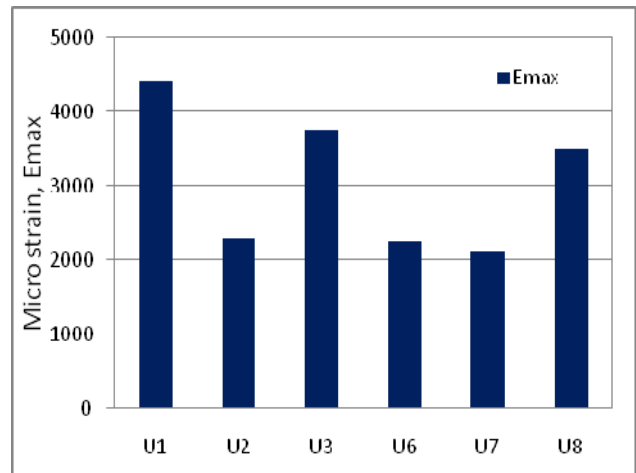

Figure 16 Maximum principal strains induced in different components of array 12×12

Figure 16 depicts the maximum values of principal corner strain induced at each component of JEDEC board of array size 12×12. The pattern shown in the figure clearly indicates that the maximum values of principal strain in components U1, U3 and U8 are much higher than components U2, U6 and U7. The difference between two groups is almost by 50%. Overall, the strains induced in PCB board can be ranked as U1>U3>U8>U2>U6>U7. It is fairly clear that U1, U3 and U8 are going to fail first than U2, U6 and U7. Therefore U1, U3 and U8 are more important components in JEDEC board. In the subsequent analysis only results from U1, U3 and U8 are presented in this paper.
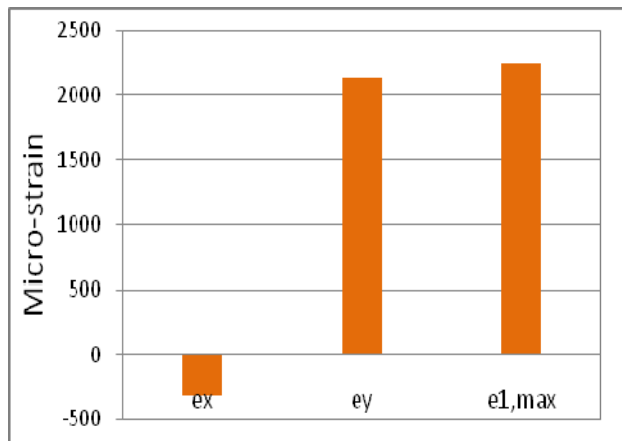
5.2 Effect of Array Size

In previous section, it is discovered that U1 has maximum board corner strain. Here its behavior has been tested for different array sizes. Figure 17 plots the maximum principal strain and maximum x-strain at U1 in array sizes from 6×6 to
28×28. As array size increases beyond 20×20 (package size 10mmx10mm), strain decreases in PCB board. This nature is found not only with maximum principal strain but the same as with strain in x-direction.
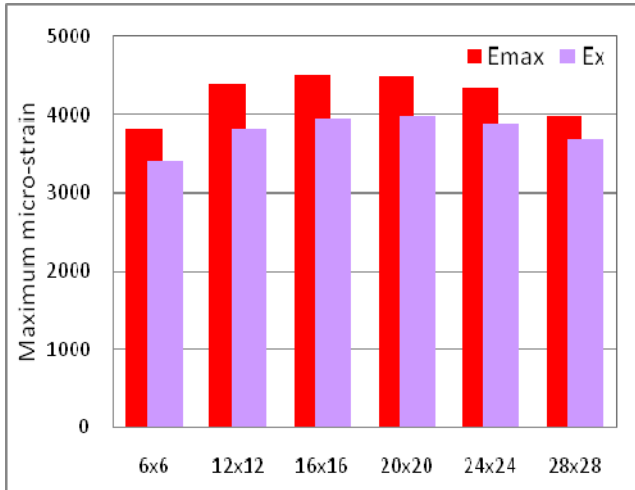

Figure 17 Plot for maximum principal strains and strains in X-direction at U1 of different arrays

Now let us look at behavior of strains induced at U3 and U8 components with different array sizes in JEDEC board, as shown in Figure 18 and 19. It clearly shows the fact that with increase in array size, both principal strains and strains induced in x-direction at component U3 and U8 increase.
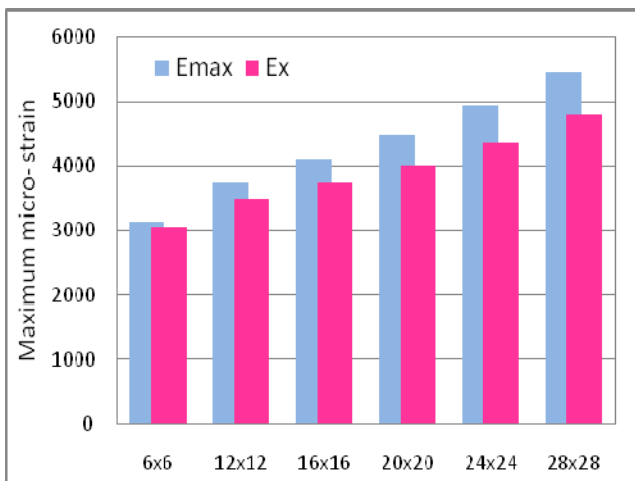

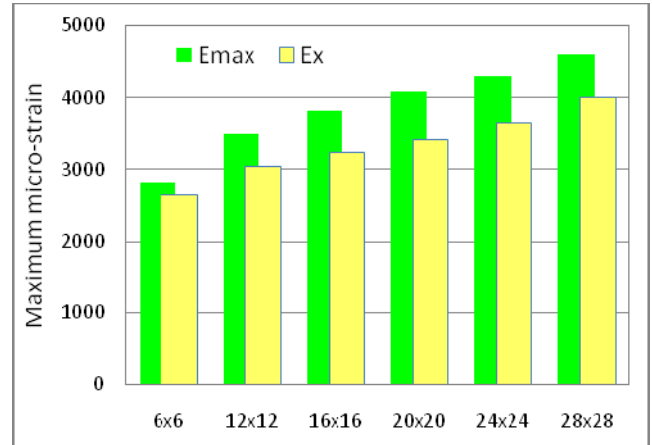Figure 18 Plot for maximum principal strains and strains in x-direction at U3 of different arrays

Figure 19 Plot for maximum principal strains and strains in x-direction at U8 of different arrays
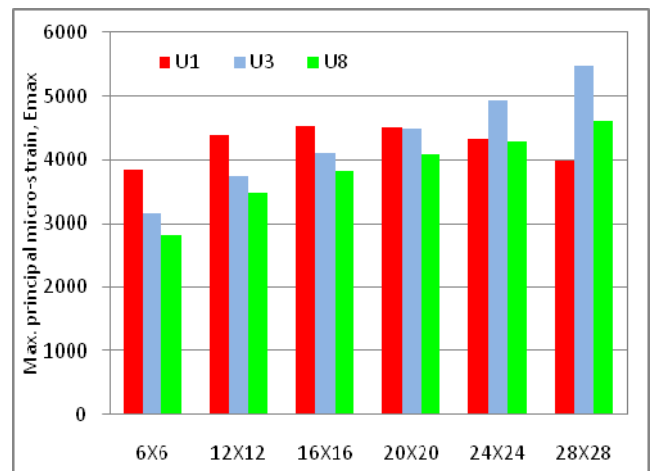

Figure 20 Plot for comparison between maximum principal strains induced at U1, U3 & U8 of different arrays

Figure 20 plots the compiled strain data for components U1, U3 and U8 for different array sizes. From this figure U1, U3 and U8 are ranked for various array sizes as shown in Table 3. It can be seen that the rank changes with array size. This implies that with large array size, the first failure may shift from the component U1 to U3 and U8.

Table 3 Ranking of U1, U3 and U8 based on maximum principal strain with different sizes

Array Size	Rank
6x6	U1 > U3 > U8
12x12	U1 > U3 > U8
16x16	U1 > U3 > U8
20x20	U1 > U3 > U8
24x24	U3 > U1 > U8
28x28	U3 > U8 > U1

6. Strain Comparison between Global and Local Models

To check whether global/local model built is accurate or not, corner strains from global model and local model with array size of 12 are compared in Figure 21. Figure 22 is a time strain history plot for U1, U3 and U8 components for 12×12 global and local models. It validates that corner strains in local and global model are same.
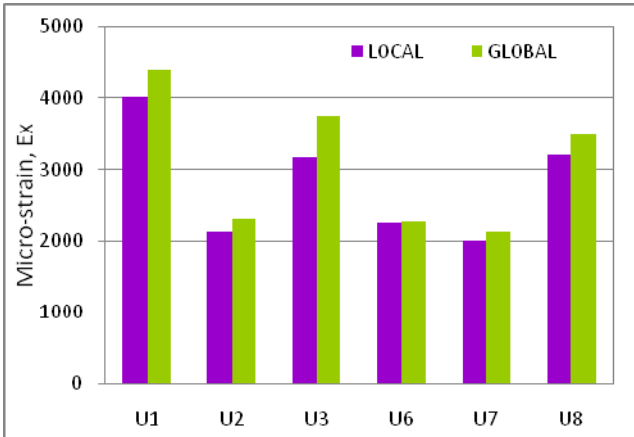

Figure 21 Plot for comparison between corner strains induced in local and global model of array 12×12 in x-direction
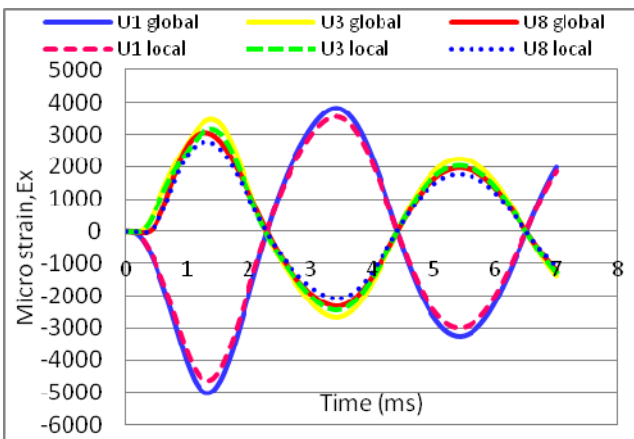

Figure 22 Comparison between time strain history plot for global and local model

7. Solder Joint Stress and Experimental Validation

Since the stresses and strains cannot be found in solder balls, strain measurement at PCB at corner locations are considered as a tool to calculate the stress level in solder balls. It is recognized that board strain at location near the package corner would determine the limit of PCB loading, regardless of package types and loading conditions. Figure 23 shows the correlation between maximum principal corner strain and maximum peeling stress for different components in 12×12 array WLP. It is noticed that the relation between board strain and peeling strees in critical layer holds very well.
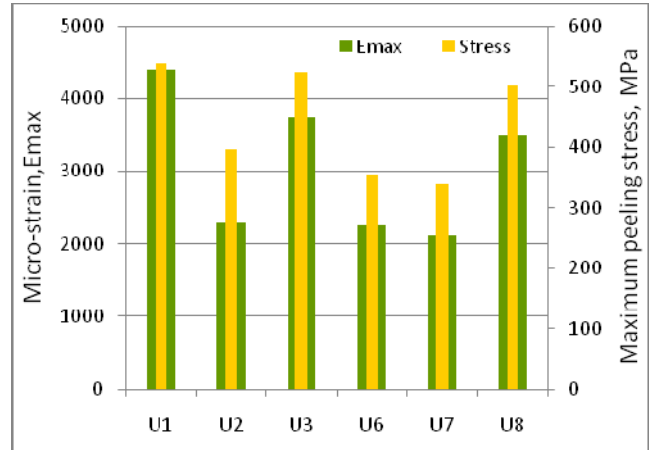

Figure 23 Plot for correlation between maximum principal strains and maximum peeling stresses in different components of array 12×12
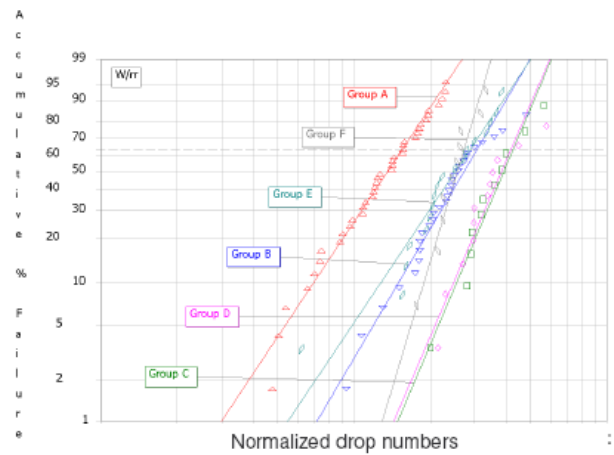

Figure 24 Weibull Plots for a 12x12 array 0.5mm Pitch WLP Components [?]

Figure 24 shows the experimental data (Weibull plots) of a 0.5mm pitch WLP for JEDEC JESD22-B111 standard test board during the drop test [6]. It is noted from this figure that component in group A (U1, U5, U11 and U15) failed first during the drop test. The failure of component by this experimental data is as U1>U3 or U8>U2>U6>U7, which is well matched with finite element analysis result data given in Figure 23.

8. Effect of Array Size on Solder Joint Stress

Further investigation is done to find out the effect of array size on maximum peeling stress generated in critical layer which causes the failure of solder ball. At first, individual behavior of each component is checked for different array sizes and then these are ranked based on maximum peeling stress. Figure 25 shows the maximum peeling stress in critical layer of solder ball at component U1 in different array sized WLPs. The trend is very clear in the figure that up to 20×20 array maximum peeling stress increases but it decreases afterwards.
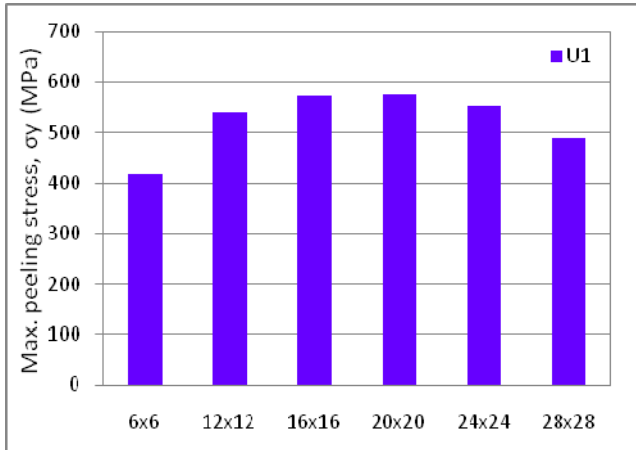
Figure 25 Plot for maximum peeling stresses at U1 of different array sized WLPs

Figure 26 and Figure 27 are the patterns of maximum peeling stresses induced in critical layers of solder balls of WLP models of various array sizes. There is continuous increase in peeling stress at both U3 and U8 components when chip size increases.
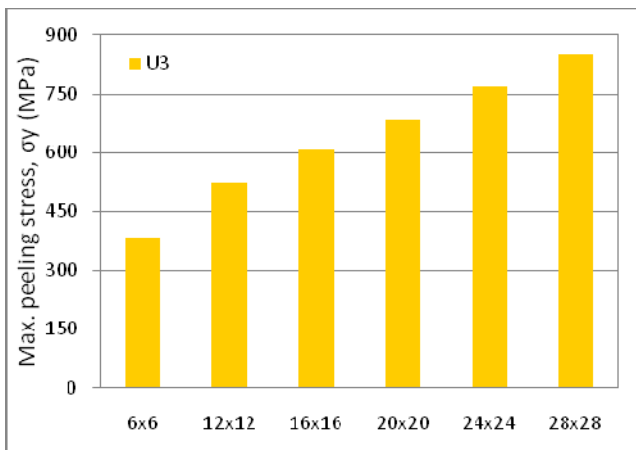

Figure 26 Plot for maximum peeling stresses at U3 of different array sized WLPs
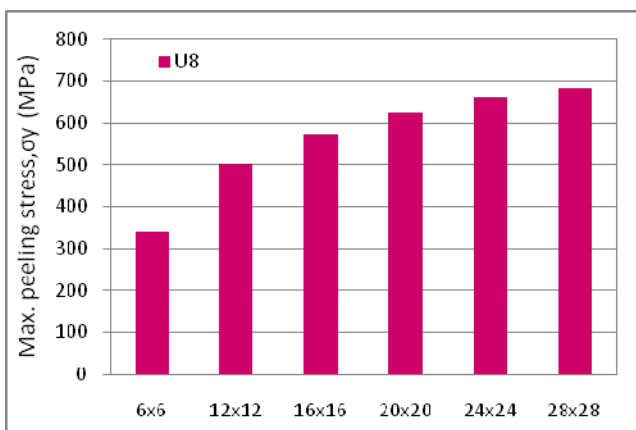

Figure 27 Plot for maximum peeling stresses at U8 of different array sized WLPs
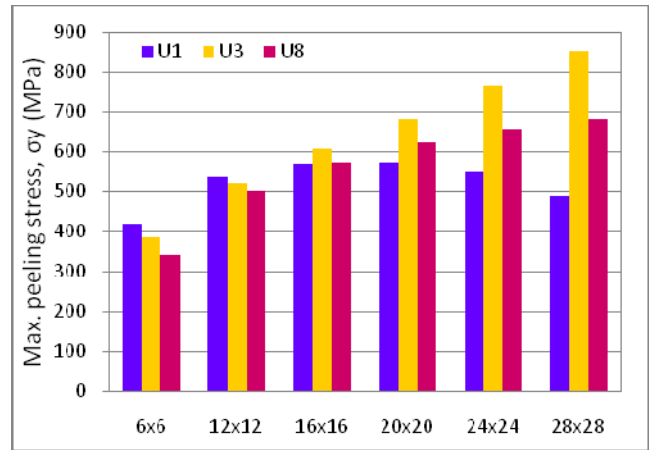

Figure 28 Comparison between maximum peeling stresses at U1, U3 & U8 of different array sized WLPs

Figure 28 shows the comparison between maximum peeling stresses produced at U1, U3 and U8 in various WLPs of array size from 6×6 to 28×28. Using this figure, Table 4 is generated which depicts the trend of failure of components in different array sized WLPs. It can be seen that the first failure location will shift from U1 location to U3 location when array size increases. Compared to the Table 3, it is found that the correlation does not hold based on the ranking from strain and the ranking from stress. This means that although corner strain is a good indicator for solder joint failures, but exact correlation with solder joint stress is more complicated.

Table 4 Failure trend in components for different array sizes

Array size	Order in which components fail		
	1st	2nd	3rd
6×6	U1	U3	U8
12×12	U1	U3	U8
16×16	U3	U8	U1
20×20	U3	U8	U1
24×24	U3	U8	U1
28×28	U3	U8	U1

9. Conclusions

In this study, large array WLP drop test reliability has been studied with an integrated testing, finite element modeling and failure analysis approach. For standard JEDEC drop test, it has been found that corner component group (group A) failed first for 12×12 array packages. This unexpected result is different from previously reported failure data of BGA packages. The high failure rate of group A is mainly due to the effect of mounting screws rather than the intrinsic strength of the package. For a given WLP, corner balls always fail first during drop test. The crack initiates at inner side of the solder joint and propagate towards the opposite side. The primary failure is always on the intermetallic compound (IMC) at WLP side. It has been found that drop reliability significantly decreases with array size increases.

Novel finite element modeling approach has been developed in this paper to correlate with experimental data. The direct acceleration input method has been applied to apply impulse loading effectively. IMC layer has been created in the local model to capture dynamics solder joint stresses accurately. The finite element model was validated with experimental board strain data, and frequency analysis. In-plane principal strain at corner locations and maximum peeling stress in IMC at critical solder joints are used to correlate with experimental data. Excellent agreement was reached to predict the failure rate of components in each group.

For different array sizes board strains have been studied at different component locations. At U1, board strain increases when array size increases from 6×6 to 20×20. However, board strain starts to decrease beyond 20×20 arrays. U3 and U8 board strain keeps increasing as array size increases. Similar trends have been found for peeling stress at IMC in critical solder joints. This implies that for very large array size package, U3 and U8 will first earlier than U1, which are consistent with experimental data of BGA packages.

The orders to fail for different components are different based on board strain and peeling stress, respectively. The correlation between solder ball stresses and board strains is investigated by results from local model and global model of 12×12 arrays respectively. It is found that board strain is able to capture change of solder ball stress when chip size is changed. But some caution must be taken while using board strain alone as parameter to analyze solder joint performance under drop impact.

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